

**JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY-GURUJADA VIZINAGARAM**  
**III B. Tech II Semester Supplementary Examinations, November -2025**  
**VLSI DESIGN**  
**(ECE)**

Time: 3 hours

Max. Marks: 70

Answer any **FIVE** Questions **ONE** Question from **Each unit**  
All Questions Carry Equal Marks

		<b><u>UNIT-I</u></b>	
1.	a)	With a neat diagram, explain the working of a BiCMOS inverter and discuss its advantages.	[7M]
	b)	Compare the characteristics of depletion, enhancement, and complementary pull-up configurations in inverter design.	[7M]
		(OR)	
2.	a)	Differentiate between CMOS and BiCMOS logic families based on performance and fabrication aspects.	[7M]
	b)	Draw and explain the layout (stick diagram) of two-input CMOS NAND and NOR gates.	[7M]
		<b><u>UNIT-II</u></b>	
3.	a)	Describe the various MOSFET scaling techniques and analyze their influence on device parameters.	[7M]
	b)	Discuss short-channel effects and their implications on MOSFET performance.	[7M]
		(OR)	
4.	a)	Explain the challenges associated with driving large capacitive loads in VLSI circuits and suggest design solutions.	[7M]
	b)	Define sheet resistance and area capacitance. Explain their role in interconnect modeling with suitable diagrams.	[7M]
		<b><u>UNIT-III</u></b>	
5.	a)	Explain the operation of a Common Source amplifier and compare it with Common Gate configuration.	[7M]
	b)	Discuss the design and operation of current mirrors used as current sources in analog VLSI.	[7M]
		(OR)	
6.	a)	Explain the different operating regions of a MOSFET with suitable transfer characteristics.	[7M]
	b)	Draw and describe the operation of a single-stage amplifier using an active load.	[7M]
		<b><u>UNIT-IV</u></b>	
7.	a)	Explain the implementation of logic functions using pass transistor logic with an example.	[7M]
	b)	Discuss the design of a two-phase clock generator using flip-flops and illustrate its timing diagram.	[7M]
		(OR)	
8.	a)	Explain the operation of clocked sequential circuits such as shift registers and counters.	[7M]
	b)	Describe various clocking strategies and their importance in synchronous VLSI design.	[7M]
		<b><u>UNIT-V</u></b>	
9.	a)	What are Field Programmable Gate Arrays (FPGAs)? Explain their internal architecture and operation.	[7M]
	b)	Describe the impact of short-channel effects and methods to mitigate them in modern VLSI devices.	[7M]
		(OR)	
10.	a)	Explain how pass transistors are used for interconnect programming in FPGA architecture.	[7M]
	b)	Write short notes on emerging transistor technologies such as Tunnel FETs (TFETs) and FinFETs.	[7M]